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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,577	02/23/2004	Donald Thomas McGrath	RD-27645-2	9571

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John S. Beulick
Armstrong Teasdale LLP
Suite 2600
One Metropolitan Square
St. Louis, MO 63102

EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2817	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,577	MCGRATH, DONALD THOMAS	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-29* is/are pending in the application.

4a) Of the above claim(s) *27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26, 28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim 27 has been withdrawn from consideration because it is directed toward the combination of a BFL and a chopping circuit that was the subject of the previous parent application serial number 09/682,863. Note the restriction requirement in 09/682,863. The search for the combination of the BFL and the chopping circuit now present was not required for the BFL circuit. This places an additional burden on the examiner. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 27 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP 821.03.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Biard 4,661,726 (Biard).

Figure 4 and the relevant text of Biard discloses a buffered field effect transistor (BFL) level-shifting/inverter circuit having an "inverter stage" input "IN", a first depletion mode inverter that receives i.e. is responsive to the "inverter stage" input IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage. The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34. The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 of Biard recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs, but Biard is also very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors (MOSFET's)...(emphasis added)." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and includes depletion mode MOSFETs. Biard is silent

on the type of depletion mode MOSFET, i.e. NMOS or PMOS. NMOS and PMOS depletion mode MOSFETs are conventional forms of depletion mode MOSFETs.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used depletion mode NMOS transistors for the transistors of Biard because, as the Biard reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent depletion mode FET such as the conventional depletion mode MOSFET.

As to the newly added claim language, the device of Biard is capable of performing the newly recited function and as such Biard meets these newly added limitations (See In re Schreiber, 128 F. 3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997).

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Biard 4,661,726 (Biard) in further in view of Tohyama 4,810,907 (Tohyama) and Alok et al. 6,559,068 (Alok).

Figure 4 and the relevant text of Biard discloses a buffered field effect transistor (BFL) level-shifting/inverter circuit having an input "IN", a first depletion mode inverter that receives the IN signal at a depletion mode MOSFET 30, and a buffered field effect transistor logic stage. The buffered field effect transistor logic stage has a first depletion mode MOSFET 32 and a second depletion mode MOSFET 37. A voltage drop or what is commonly called a level shifter is connected between the first and second transistors and is composed of elements like 33, 34. The node between element 32 and 33 forms a first output and the node between element 37 and 36 forms a second output. It is important to note that column 1, around line 50 of Biard recites that the logic gates of the invention "will therefore be described in terms of such logic gates" i.e. MESFETs, but Biard is also very specific that "[t]hose skilled in the art will readily perceive that the invention (which includes the BFL of Figure 4) may be used with any logic gate utilizing depletion mode FET's. Such FET's may be metal oxide semiconductor field effect transistors (MOSFET's)...(emphasis added)." Thus the Figure 4 embodiment is clearly applicable to MOSFETs and includes depletion mode MOSFETs. Biard is silent on the type of depletion mode MOSFET, i.e. NMOS or PMOS. Alok discloses that silicon carbide NMOS and PMOS depletion mode MOSFETs formed on a silicon carbide substrate are conventional forms of depletion mode MOSFETs (See entire reference.). Alok also teaches the motivation for use of Silicon Carbide transistors that includes that they are ideal for "high voltage, high frequency and high temperature" (See column 1, around line 33).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used silicon carbide depletion mode NMOS transistors formed on a silicon carbide substrate for the transistors of Biard because, as the Biard reference is silent on the exact depletion mode FET used one of ordinary skill in the art would have been motivated to use any art-recognized equivalent depletion mode FET such as the conventional silicon carbide depletion mode NMOS MOSFET formed on a silicon carbide substrate. Additionally one of ordinary skill would have been motivated to make the combination because of the higher voltage handing, the higher frequency capabilities and the higher temperature handing capabilities as compared to conventional Si based MOS devices as taught by Alok. Silicon carbide MOSFETs are better FETs.

Biard is silent on the use of resistor(s) for the voltage drop circuit.

Tohyama shows that the resistor, the diode and the "diode connected " FET like that of Biard are all art-recognized equivalent voltage drop circuits for use in BFT's.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the voltage drop circuit of Biard with a resistor because two voltage drop circuits are well known to be equivalent in the art as taught by Tohyama.

Because the combination made obvious above includes depletion mode NMOS transistors, this circuit being the same as that claimed is configured to operate with a negative direct current bias on each of the gates with respect to the associated channel.

Response to Arguments

Applicant's arguments filed 10-19-2006 have been fully considered but they are not persuasive. Applicant is in effect arguing that Biard does not intend to use the use the node between the elements 32 and 33 as an output. One cannot determine this from Biard. But more importantly, the examiner cited the Schreiber case. Most certainly in the instant case the node between elements 32 and 33 could be used as an output. What is being claimed is the structure of the "BFL". It is not a method for buffering and most certainly any node in an electrical circuit will have a voltage associated with it or signal associated with it and this signal can be measured i.e. it is an output. For example an oscilloscope could be connected to any point in the circuit to see what the signal is and this connection is an output. MEPP 2114 is very clear

that claims drawn to structure must be distinguished by structure. A node can function as an output and hence is an output.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
January 20, 2006
July 4, 2006
January 7, 2007

Michael B Shingleton
Primary Examiner
Group Art Unit 2817